

Amendments to the Claims

1. *(Currently Amended)* A circuit arrangement comprising at least one circuit component ~~(304)~~ at which a load is applied that can vary during operation of said circuit arrangement, wherein said circuit arrangement comprises:
 - a. load determination means ~~(40)~~ for determining a load applied at said at least one circuit component ~~(304)~~; and
 - b. adjusting means ~~(50)~~ for adjusting drive capacity of said at least one component ~~(304)~~ responsive to said determination means.
2. *(Currently Amended)* A circuit arrangement according to claim 1, wherein said determination means ~~(40)~~ is configured to determine said load based on a configuration information loaded to said circuit arrangement.
3. *(Currently Amended)* A circuit arrangement according to claim 2, wherein said configuration information is stored in a configuration memory ~~(40)~~.
4. *(Currently Amended)* A circuit arrangement according to ~~claim 2 or 3~~ claim 2, wherein said configuration information comprises a configuration bit stream defining at least one of an input load and an output load of said at least one component ~~(304)~~.
5. *(Currently Amended)* A circuit arrangement according to ~~any one of the preceding claims~~ claim 1, wherein said adjusting means ~~(50)~~ is configured to vary a buffer or a buffer number of said at least one component ~~(304)~~.
6. *(Currently Amended)* A circuit arrangement according to claim 5, wherein said adjusting means ~~(50)~~ is configured to switch on or off buffers ~~(304)~~ or buffer sections ~~(341 to 346)~~ responsive to said determination means ~~(40)~~.
7. *(Currently Amended)* A circuit arrangement according to ~~claim 5 or 6~~ claim 5, wherein said adjusting means ~~(50)~~ is adapted to generate at least one control signal ~~(CMN)~~ for switching on or off said buffer sections ~~(3041 to 3046)~~.

8. *(Currently Amended)* A circuit arrangement according to claim 6, wherein said adjusting means ~~(50)~~ is adapted to derive said control signal only from a most significant bit signal of a selection signal obtained from said determination means 50.

9. *(Currently Amended)* A circuit arrangement according to ~~any one of the preceding claims~~ claim 1, wherein said adjusting means ~~(50)~~ is configured to vary a threshold voltage of circuit elements of said circuit arrangement.

10. *(Currently Amended)* A circuit arrangement according to claim 9, wherein said adjusting means ~~(50)~~ is adapted to change at least one bias voltage ~~(VPW, VNW)~~ responsive to said determination means ~~(40)~~.

11. *(Currently Amended)* A circuit arrangement according to ~~any one of the preceding claims~~ claim 1, wherein said circuit arrangement is a field programmable gate array device.

12. *(Currently Amended)* A method of controlling power consumption of a circuit arrangement, said method comprising the steps of:

- a. determining a load applied at at least one circuit arrangement; and
- b. adjusting a drive capacity of said at least one component ~~(304)~~ responsive to said determination step.